Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A**
2. **1B**
3. **1Y**
4. **2A**
5. **2B**
6. **2Y**
7. **GND**
8. **3Y**
9. **3A**
10. **3B**
11. **4Y**
12. **4A**
13. **4B**
14. **VCC**

**.051”**

**13 12 11 10 9**

**3 4 5**

**14**

**1**

**2**

**8**

**7**

**6**

**MASK**

**REF**

**ACT86**

**.051”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: VCC or FLOAT**

**Mask Ref: ACT86**

**APPROVED BY: DK DIE SIZE .051” X .051” DATE: 6/6/22**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 74ACT86**

**DG 10.1.2**

#### Rev B, 7/1